ANALOG DEVICES

50 dB GSM PA Controller

Preliminary Technical Data

AD8311

FEATURES

Complete RF detector/controller function
>50 dB range at 0.9 GHz (–49 dBm to +2 dBm re 50 Ω)
Accurate scaling from 0.1 GHz to 2.5 GHz
Temperature-stable linear-in-dB response
Log slope of 23.6 mV/dB, intercept at –59.7 dBm at 0.9 GHz
True integration function in control loop
Low power: 20 mW at 2.7 V, 38 mW at 5 V

APPLICATIONS

Single, dual, and triple band mobile handset (GSM, DCS, EDGE)
Transmitter power control

PRODUCT DESCRIPTION

The AD8311 is a complete low cost subsystem for the precise control of RF power amplifiers operating in the frequency range 0.1 GHz–2.5 GHz and over a typical dynamic range of 50 dB. It is intended for use in cellular handsets and other battery-operated wireless devices. The log amp technique provides a much wider measurement range and better accuracy than controllers using diode detectors. In particular, its temperature stability is excellent over a specified range of –40°C to +85°C.

Its high sensitivity allows control at low signal levels, thus reducing the amount of power that needs to be coupled to the detector. For convenience, the signal is internally ac-coupled. This high-pass coupling, with a corner at approximately 0.016 GHz, determines the lowest operating frequency. Thus, the source may be dc grounded.

The AD8311 provides a voltage output, VAPC, that has the voltage range and current drive to directly connect to most handset power amplifiers' gain control pin. VAPC can swing from 250 mV above ground to within 200 mV below the supply voltage. Load currents of up to 6 mA can be supported.

The setpoint control input is applied to pin VSET and has an operating range of 0.25 V–1.4 V. The associated circuit determines the slope and intercept of the linear-in-dB measurement system; these are nominally 23.6 mV/dB and –59.7 dBm at 0.9 GHz. Further simplifying the application of the AD8311, the input resistance of the setpoint interface is over 100 MΩ, and the bias current is typically 0.5 µA.

The AD8311 is available in a 6-lead wafer-level chip scale package, 1.0 mm x 1.5 mm, and consumes 7.6 mA from a 2.7 V to 5.5 V supply.

FUNCTIONAL BLOCK DIAGRAM

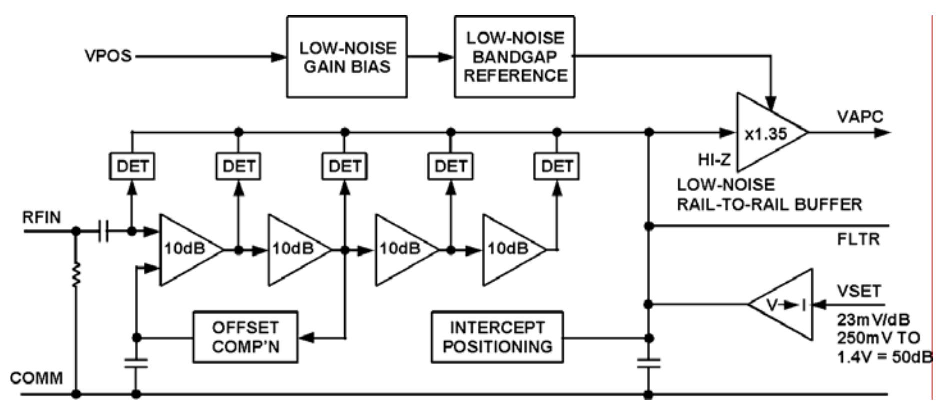

Figure 1.

Rev. PrA **04/18/2005**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

Specifications

Table 1. V_S = 2.7 V, Freq = 0.1 GHz, T = 25°C, 52.3 Ω termination on RFIN, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	RFIN (Pin 6)				
Specified Frequency Range		0.1		2.5	GHz
Input Voltage Range	±1 dB Log Conformance, 0.1 GHz	1.4		282	mV rms
Equivalent dBm Range		−44		+2	dBm
MEASUREMENT MODE	VAPC (Pin 2) to VSET (Pin 3) with inversion stage, Sinusoidal Input Signal				
f = 0.1 GHz					
Input Impedance	No termination resistor		2100 || 790		Ω || pF
± 1 dB Dynamic Range	T_A = +25°C		47		dB
	−40°C < T_A < +85°C		46		dB
Maximum Input Level	± 1 dB Error		+2.5		dBm
Minimum Input Level	± 1 dB Error		-44.5		dBm
Slope		tbd	23.8	tbd	mV/dB
Intercept		tbd	-58.9	tbd	dBm
Output Voltage - High Power In	P_{IN} = −10 dBm	tbd	tbd	tbd	V
Output Voltage - Low Power In	P_{IN} = −40 dBm	tbd	tbd	tbd	V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		tbd		dB/°C
	−40°C ≤ T_A ≤ +25°C		tbd		dB/°C
f = 0.9 GHz					
Input Impedance	No termination resistor		370 || 110		Ω || pF
± 1 dB Dynamic Range	T_A = +25°C		51		dB
	−40°C < T_A < +85°C		50		dB
Maximum Input Level	± 1 dB Error		+3		dBm
Minimum Input Level	± 1 dB Error		-48		dBm
Slope			23.6		mV/dB
Intercept			-59.7		dBm
Output Voltage - High Power In	P_{IN} = −10 dBm		tbd		V
Output Voltage - Low Power In	P_{IN} = −40 dBm		tbd		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		tbd		dB/°C
	−40°C ≤ T_A ≤ +25°C		tbd		dB/°C
f = 1.9 GHz					
Input Impedance	No termination resistor		180 || 50		Ω || pF
± 1 dB Dynamic Range	T_A = +25°C		43		dB
	−40°C < T_A < +85°C		42		dB
Maximum Input Level	± 1 dB Error		-5		dBm
Minimum Input Level	± 1 dB Error		-48		dBm
Slope			22.7		mV/dB
Intercept			-60.8		dBm
Output Voltage - High Power In	P_{IN} = −10 dBm		tbd		V
Output Voltage - Low Power In	P_{IN} = −40 dBm		tbd		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		tbd		dB/°C
	−40°C ≤ T_A ≤ +25°C		tbd		dB/°C

Parameter	Conditions	Min	Typ	Max	Unit
f = 2.5 GHz					
Input Impedance	No termination resistor		160 || 40		Ω || pF
± 1 dB Dynamic Range	T_A = +25°C		42		dB
	−40°C < T_A < +85°C		41		dB
Maximum Input Level	± 1 dB Error		-6		dBm
Minimum Input Level	± 1 dB Error		-48		dBm
Slope			22.5		mV/dB
Intercept			-60.6		dBm
Output Voltage - High Power In	P_{IN} = −10 dBm		tbd		V
Output Voltage - Low Power In	P_{IN} = −40 dBm		tbd		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		tbd		dB/°C
	−40°C ≤ T_A ≤ +25°C		tbd		dB/°C
OUTPUT INTERFACE	VAPC (Pin 2)				
Minimum Output Voltage	VSET ≤ 150mV	0.25	0.32	0.4	V
Maximum Output Voltage	R_L ≥ 800 Ω	2.42		2.6	V
vs. Temperature	85°C, V_{POS} = 3 V, I_{OUT} =6 mA	2.54			V
General Limit	2.7 V ≤ VPOS ≤ 5.5 V, R_L = ∞		VPOS – 0.1		V
Output Current Drive	VSET = 1.5 V, RFIN = −50 dBm, Source/Sink		tbd/tbd		mA/µA
Output Noise	RF Input = 2 GHz, 0 dBm, f_{NOISE} = 100 kHz, C_{FLT} = 220 pF		170		nV/√Hz
Small Signal Bandwidth	RFIN = −10 dBm; From CLPF to VOUT		tbd		MHz
Fall Time	Input Level = off to 0 dBm, 90% to 10%		120		ns
Rise Time	Input Level = 0 dBm to off, 10% to 90%		270		ns
Slew Rate	10%–90%, 1.2 V Step (V_{SET}), Open Loop		7		V/µs
Response Time	FLTR = Open		130		ns
VSET INTERFACE	VSET (Pin 3)				
Nominal Input Range	RFIN = 0 dBm; measurement mode		tbd		V
	RFIN = –50 dBm; measurement mode		tbd		V
Logarithmic Scale Factor			tbd		dB/mV
Bias Current Source	RFIN = −10 dBm; VSET = 1.4V		tbd		µA
Input Resistance			36		MΩ
Slew Rate			tbd		V/µs
POWER INTERFACE	VPOS (Pin 1)				
Supply Voltage		2.7	tbd	5.5	V
Quiescent Current		tbd	7.6	tbd	mA
vs. Temperature	−40°C ≤ T_A ≤ +85°C		8.2	12.9	mA
Power-On Time	Time from VPOS High to V_{APC} within 1% of Final Value, V_{SET} ≤ 200 mV		tbd	tbd	µs
Power-Off Time	Time from VPOS Low to V_{APC} within 1% of Final Value, V_{SET} ≤ 200 mV		tbd	tbd	ns

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

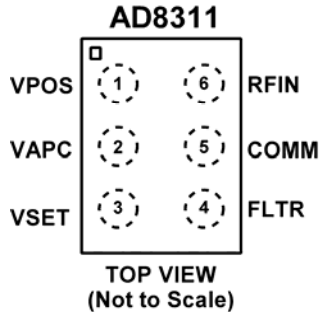

Figure 2. Pin Configuration

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	VPOS	Positive Supply Voltage: 2.7 V to 5.5 V
2	VAPC	Output. Control voltage for gain control element.
3	VSET	Setpoint Input. Nominal input range 0.25 V to 1.4 V.
4	FLTR	Integrator Capacitor. Connect between FLTR and COMM.
5	COMM	Device Common (Ground)
6	RFIN	RF Input

TYPICAL PERFORMANCE CHARACTERISTICS

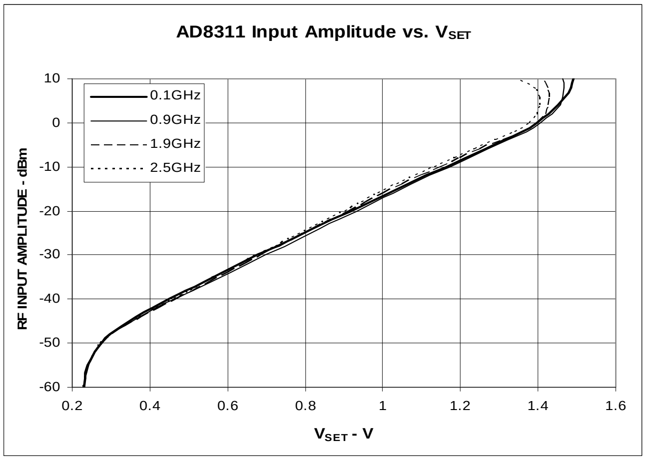

Figure 3. Input Amplitude vs. V_{SET}

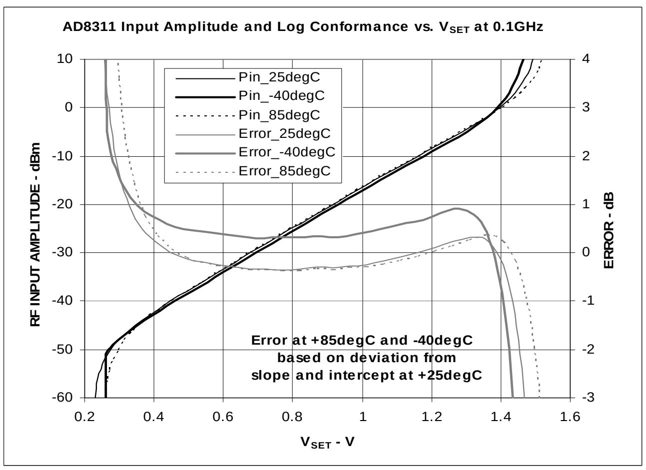

Figure 4. Input Amplitude and Log Conformance vs. V_{SET} at 0.1 GHz; −40°C, +25°C, and +85°C

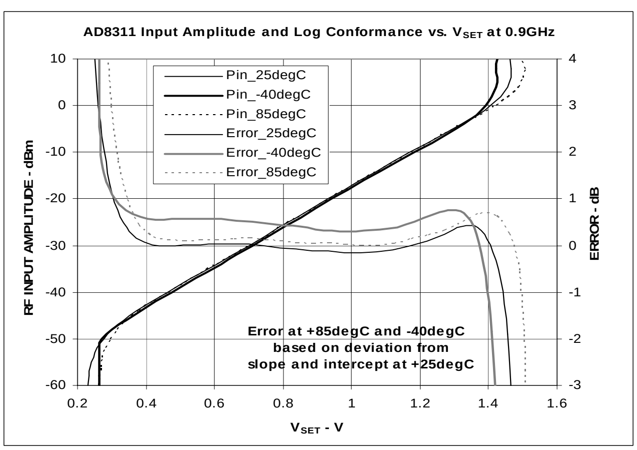

Figure 5. Input Amplitude and Log Conformance vs. V_{SET} at 0.9 GHz; −40°C, +25°C, and +85°C

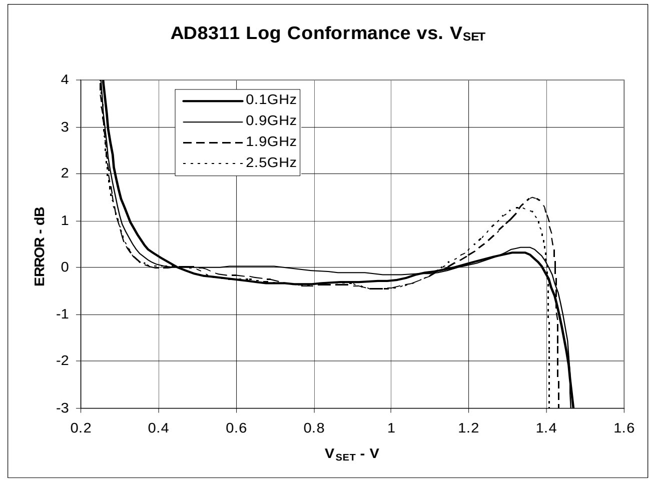

Figure 6. Log Conformance vs. V_{SET}

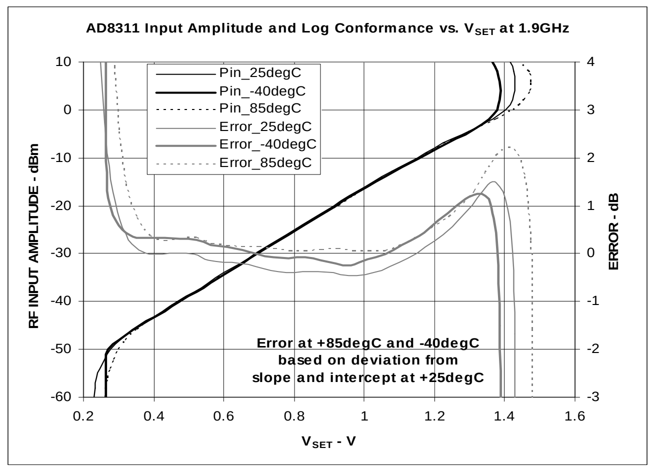

Figure 7. Input Amplitude and Log Conformance vs. V_{SET} at 1.9 GHz; −40°C, +25°C, and +85°C

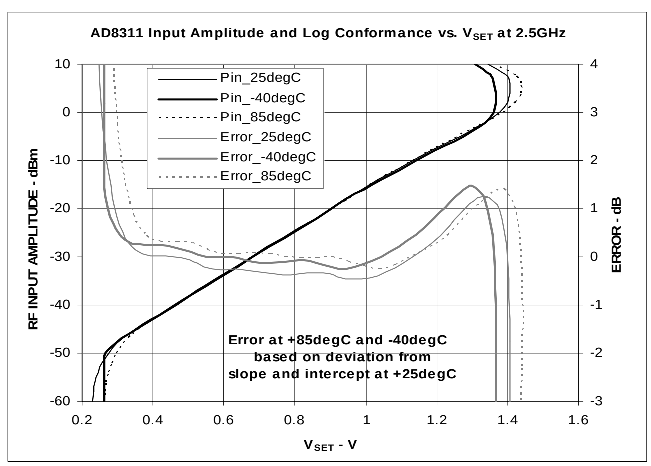

Figure 8. Input Amplitude and Log Conformance vs. V_{SET} at 2.5 GHz; −40°C, +25°C, and +85°C

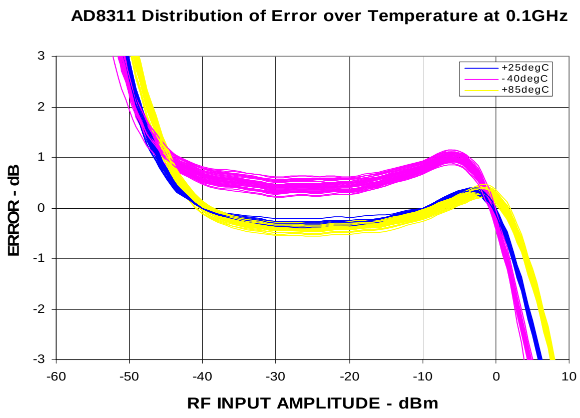

Figure 9. Distribution of Error over Temperature after Ambient Normalization vs. Input Amplitude at 0.1 GHz

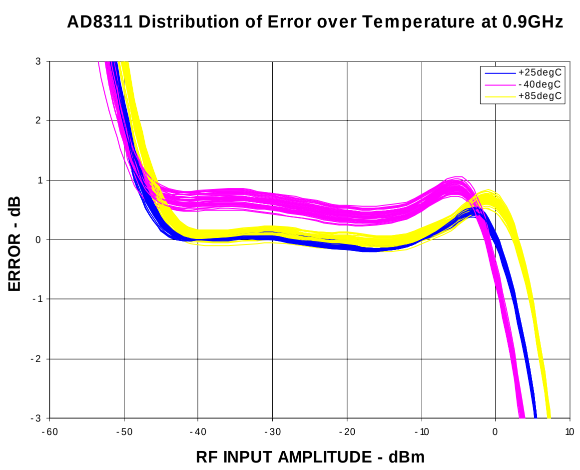

Figure 10. Distribution of Error over Temperature after Ambient Normalization vs. Input Amplitude at 0.9 GHz

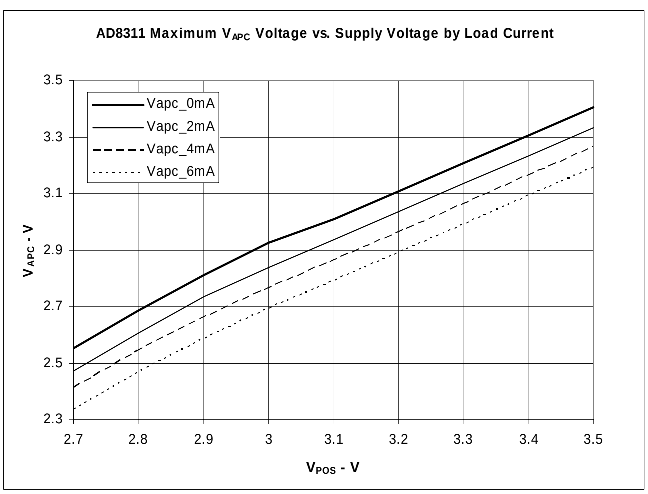

Figure 11. Maximum V_{ACP} Voltage vs. Supply Voltage by Load Current

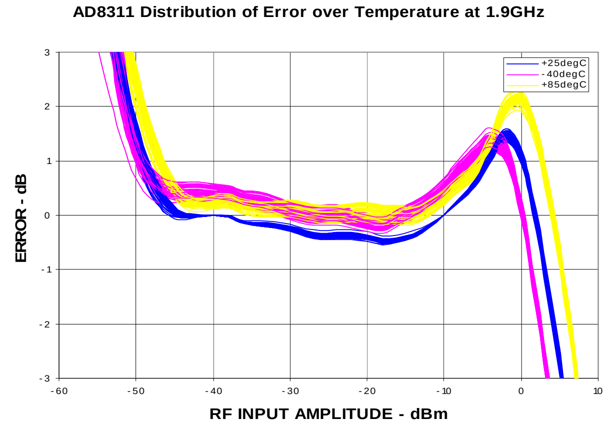

Figure 12. Distribution of Error over Temperature after Ambient Normalization vs. Input Amplitude at 1.9 GHz

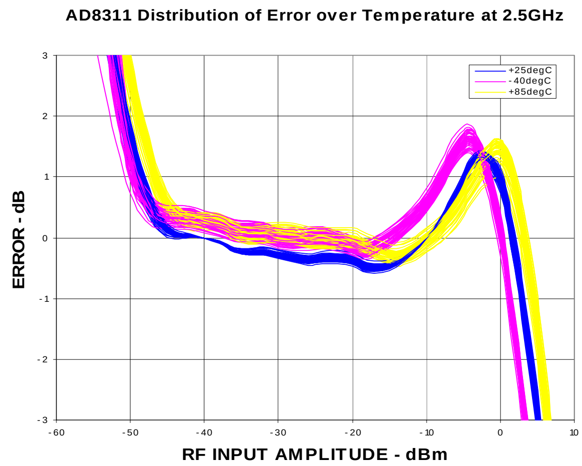

Figure 13. Distribution of Error over Temperature after Ambient Normalization vs. Input Amplitude at 2.5 GHz

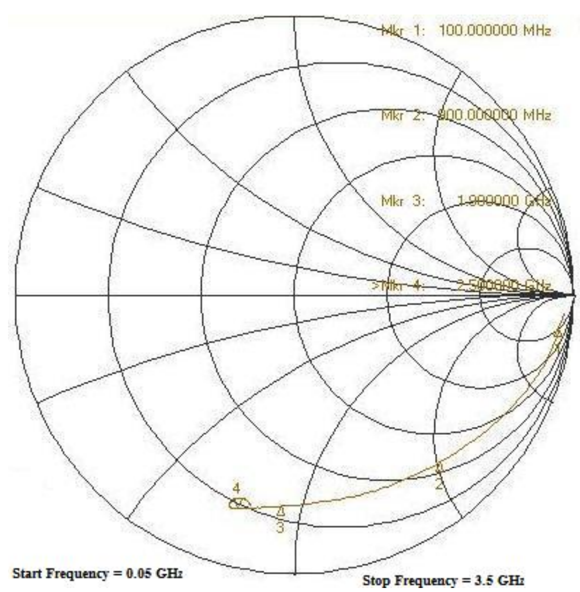

Figure 14. Input Impedance vs. Frequency; No Termination Resistor

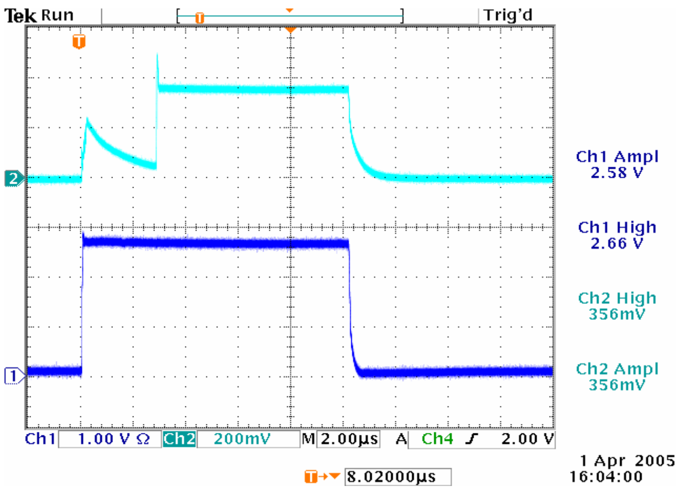

Figure 15. Power-On and –Off Response with V_{SET} Grounded

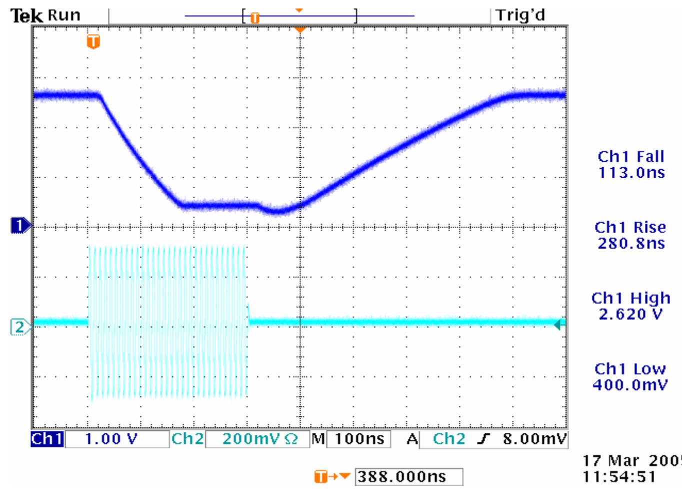

Figure 18. V_{APC} Response Time, Full-Scale Amplitude Change, Open-Loop

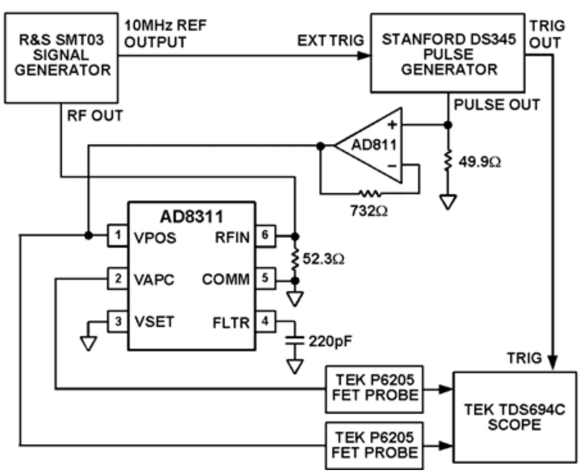

Figure 16. Test Setup for Power-On and –Off Response with VSET Grounded

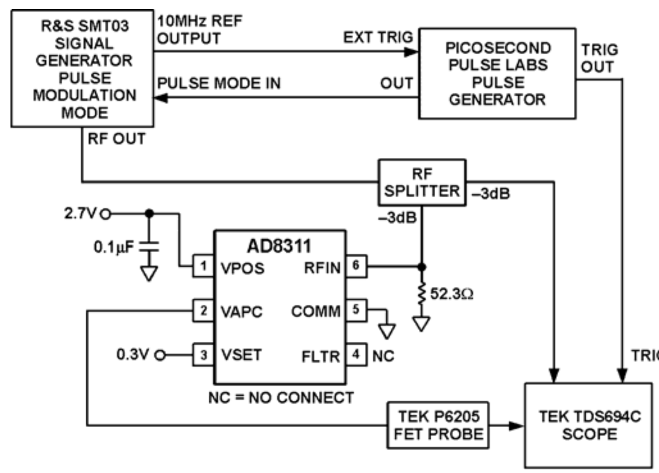

Figure 19. Test Setup for V_{APC} Response Time

Figure 17. AC Response from VSET to VAPC

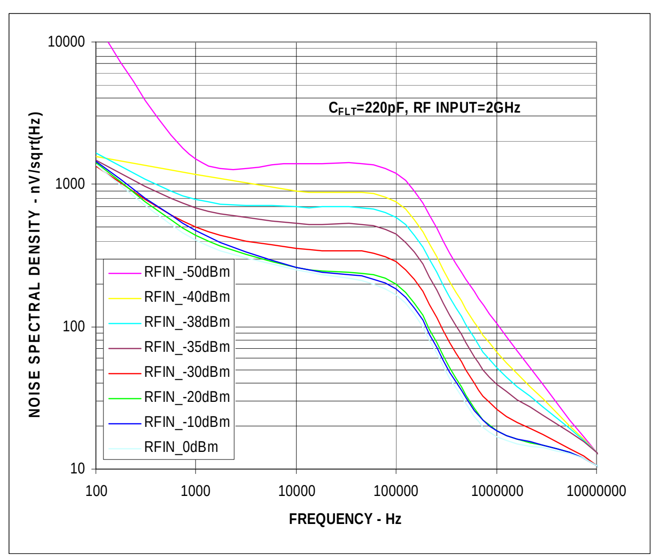

Figure 20. V_{ACP} Noise Spectral Density

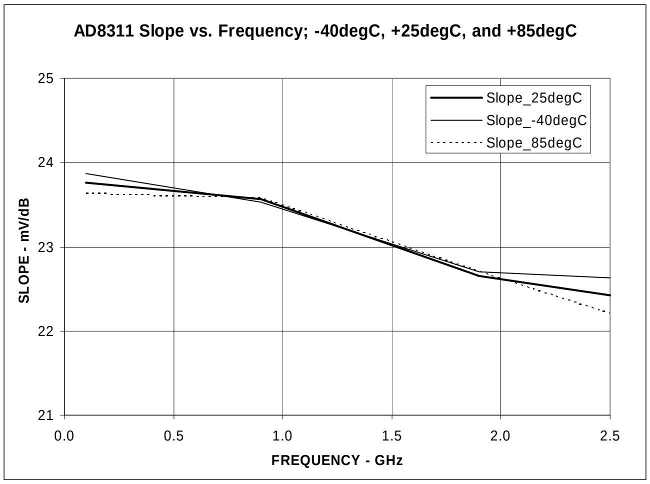

Figure 21. Slope vs. Frequency; −40°C, +25°C, and +85°C

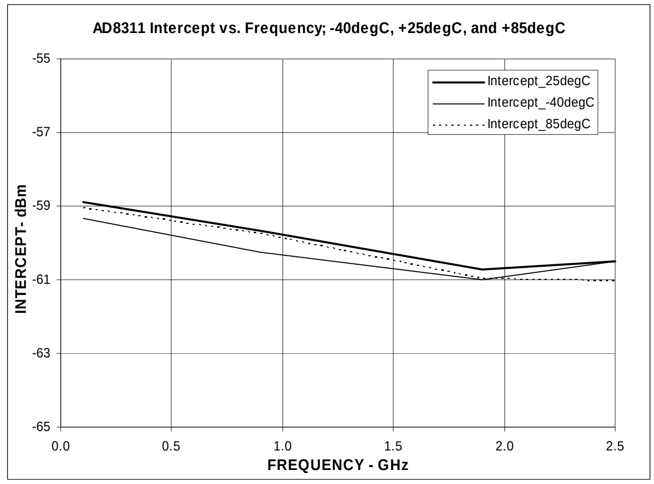

Figure 23. Intercept vs. Frequency; −40°C, +25°C, and +85°C

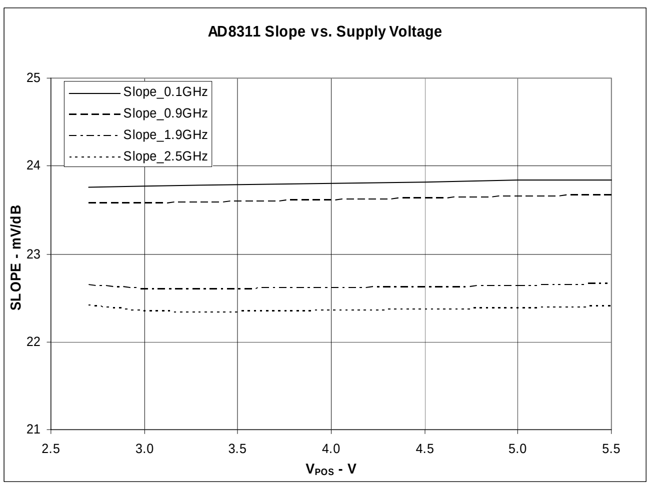

Figure 22. Slope vs. Supply Voltage; −40°C, +25°C, and +85°C

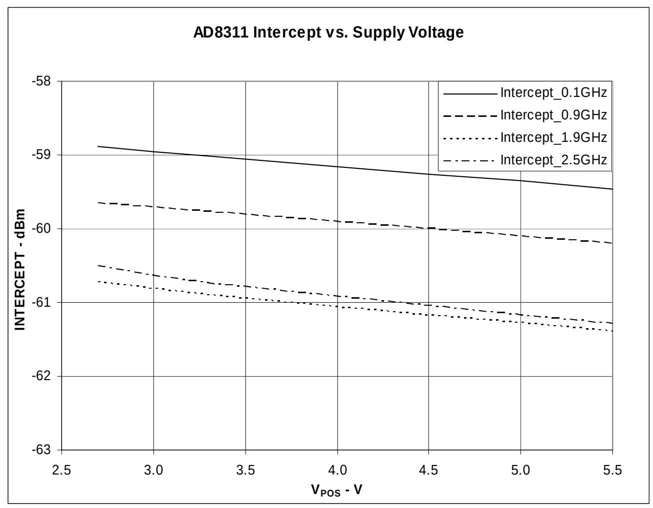

Figure 24. Intercept vs. Supply Voltage; −40°C, +25°C, and +85°C

DEVICE HANDLING

The wafer-level chip scale package consists of solder bumps connected to the active side of the die. The part is lead-free with 95.5% tin, 4.0% silver, and 0.5% copper solder bump composition. The WLCSP package can be mounted on printed circuit boards using standard surface-mount assembly techniques; however, caution should be taken to avoid damaging the die. See the AN-617 application note for additional information. WLCSP devices are bumped die, and exposed die can be sensitive to light condition, which can influence specified limits.

EVALUATION BOARD

Figure 25 shows the schematic of the AD8311 WLCSP evaluation board. The layout and silkscreen of the component and circuit sides are shown in Figure 26 to Figure 29. The board is powered by a single supply in the range, 2.7 V to 5.5 V. The power supply is decoupled by a 0.1 µF capacitor. A 100 pF capacitor provides additional supply decoupling, but is not necessary for basic operation.

Table 3 details the various configuration options of the evaluation board.

For operation in controller mode, both jumpers, J1 and J2, should be removed. The setpoint voltage is applied to V_{SET}, RFIN is connected to the RF source (PA output or directional coupler), and VAPC is connected to the gain control pin of the PA. When used in controller mode, a capacitor must be installed in C4 for loop stability (R2 must also be installed, 0Ω by default). For GSM/DCS handset power amplifiers, this capacitor should typically range from 150 pF to 300 pF.

A quasi-measurement mode (where the AD8311 delivers an output voltage that is proportional to the log of the input signal) can be implemented, to establish the relationship between V_{SET} and RFIN, by installing the two jumpers, J1 and J2. This mimics an AGC loop. To establish the transfer function of the log amp, the RF input should be swept while the voltage on V_{SET} is measured, that is, the SMA connector labeled VSET now acts as an output. This is the simplest method to validate operation of the evaluation board. When operated in this mode, a large capacitor (0.01 µF or greater) must be installed in C4 (filter capacitor) to ensure loop stability. Also, J3 must be installed to power the inverting amplifier.

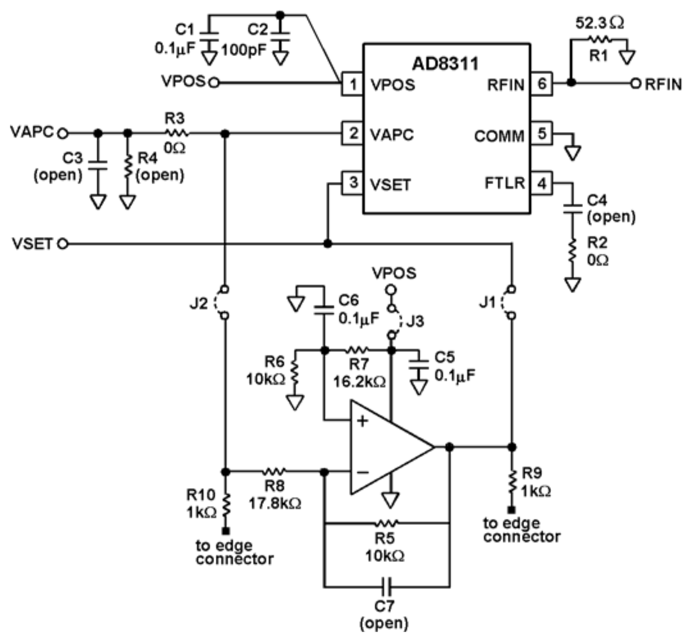

Figure 25. Evaluation Board Schematic

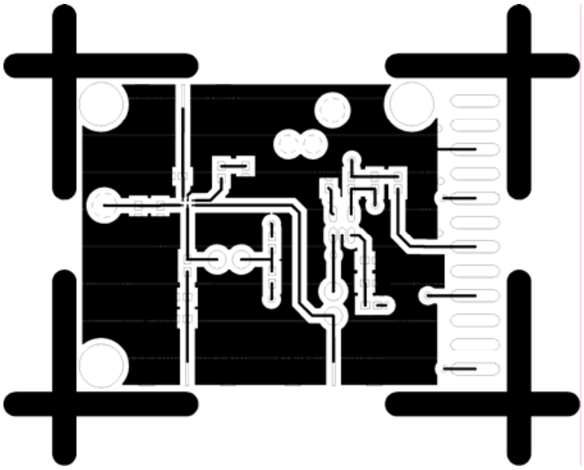

Figure 26. Layout of Component Side (WLCSP)

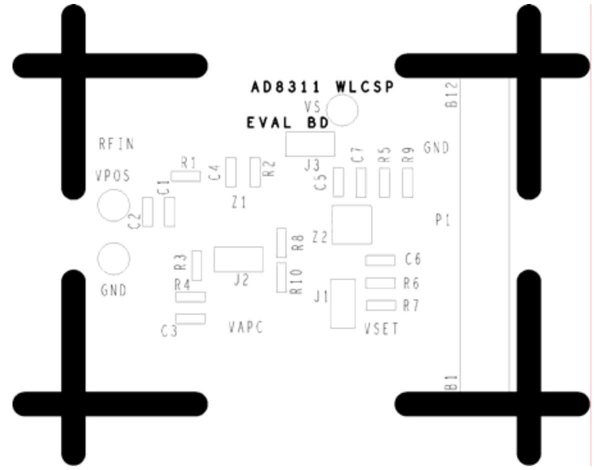

Figure 28. Silkscreen of Component Side (WLCSP)

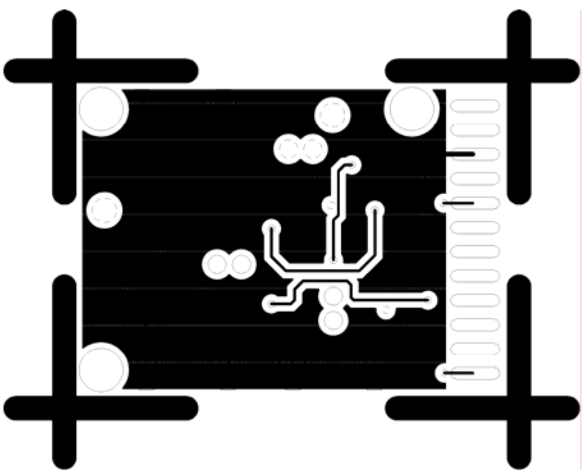

Figure 27. Layout of Circuit Side (WLCSP)

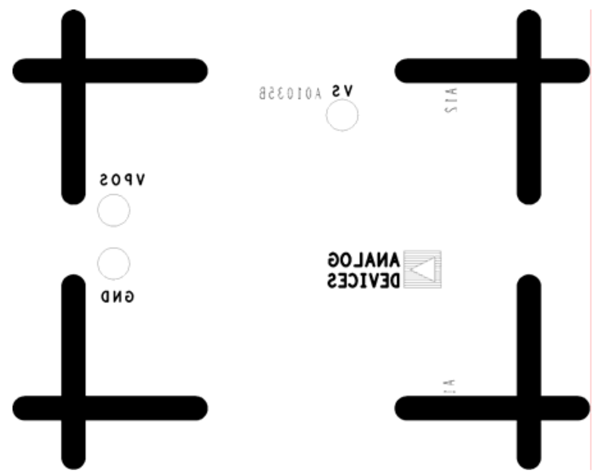

Figure 29. Silkscreen of Circuit Side (WLCSP)

Table 3. Evaluation Board Configuration Options

Component	Function	Default Condition
VPOS, GND	Supply and Ground Vector Pins	Not Applicable
R1	Input Interface: The 52.3 Ω resistor in Position R1 combines with the AD8311's internal input impedance to give a broadband input impedance of around 50 Ω. Note that the AD8311's RF input is internally ac-coupled.	R1 = 52.3 Ω (Size 0603)
R3, R4, C3	Output Interface: R4 and C3 can be used to check the response of V_{APC} to capacitive and resistive loading. R3/R4 can be used to reduce the slope of V_{APC}.	R3 = 0 Ω (Size 0603) R4 = C3 = Open (Size 0603)
C1, C2	Power Supply Decoupling: The nominal supply decoupling consists of a 0.1 µF capacitor. C2 can be used for additional supply decoupling.	C1 = 0.1 µF (Size 0603) C2 = 100 pF (Size 0603)
C4, R2	Filter Capacitor: The response time of V_{APC} can be modified by placing a capacitor between FLTR (Pin 4) and ground. The control loop phase margin can be increased by adding a series resistor.	C4 = Open (Size 0603) R2 = 0 Ω (Size 0603)
J1, J2, J3	Measurement Mode: A quasi-measurement mode can be implemented by installing J1 and J2 (connecting an inverted V_{APC} to V_{SET}) to yield the nominal relationship between RFIN and VSET. In this mode, a large capacitor (0.01 µF or greater) must be installed in C4. J3 must be installed to power the inverting amplifier.	J1, J2 = Installed J3 = Installed

OUTLINE DIMENSIONS

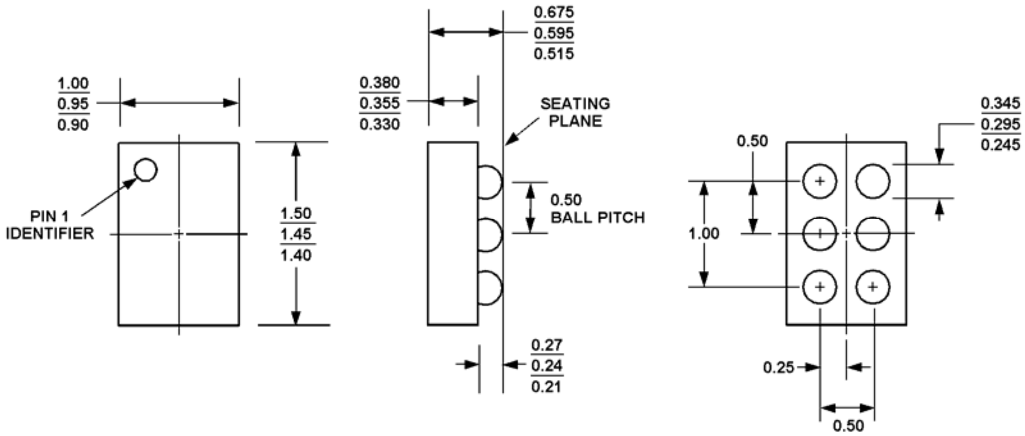

Figure 30. 6-Lead Wafer-level Chip Scale Package
Dimensions shown in mm

ORDERING GUIDE

AD8311 Products	Temperature Package	Package Description	Package Outline	Branding Information	Ordering Quantity
AD8311ACBZ-P7[1]	–40°C to +85°C	6-Lead Wafer-level Chip Scale Package, 7” Pocket Tape and Reel	CB-6	Q04	tbd
AD8311-EVAL		Evaluation Board			

[1] Z = Pb-free part.

NOTES

www.analog.com